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EECS 140 LAB

Implementation of a Counter

Due Date: February 26, 2003

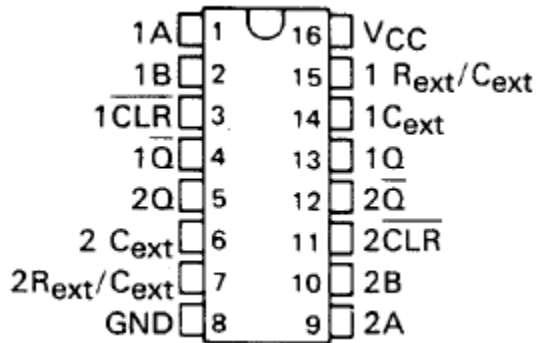
TA: James Kreycik

Objective: To create a counter that begins at 3 and counts in increasing order incrementing one integer at a time. When the output reaches 11, the counter will loop around and begin the cycle again at 3. In other words, the output is 3,4,5,...9,10,11,3,4...

## Equipment and Components

### Pin Layouts

#### 74LS123 (Monostable Multivibrator)

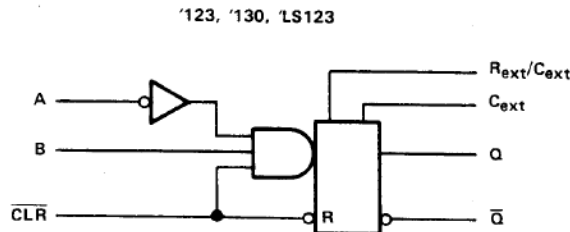


logic diagram (positive logic) (each multivibrator)

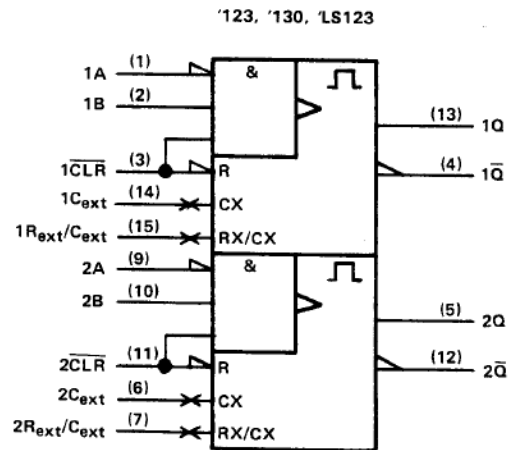
'123, '130, 'LS123  
FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	$\bar{Q}$
L	X	X	L	H
X	H	X	L $\uparrow$	H $\uparrow$
X	X	L	L $\uparrow$	H $\uparrow$
H	L	$\uparrow$	$\square$	$\square$
H	$\downarrow$	H	$\square$	$\square$
$\uparrow$	L	H	$\square$	$\square$

logic symbol $\dagger$

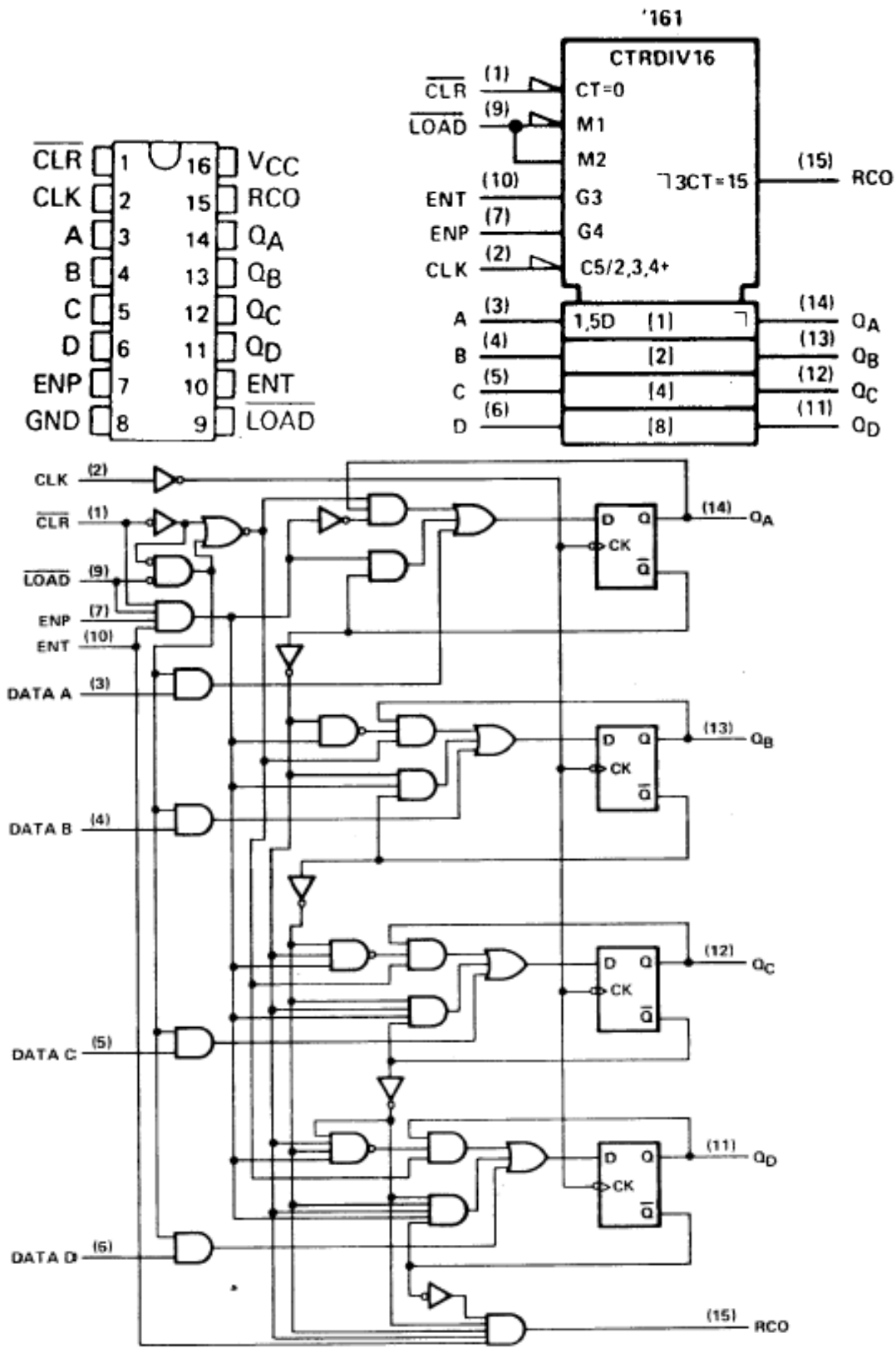


'123, '130, 'LS123

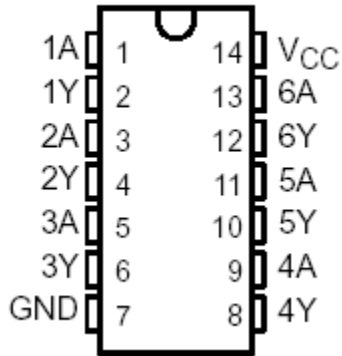


'123, '130, 'LS123

# 74LS161 (Counter)



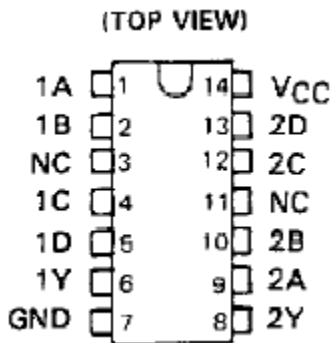
## 74LS04 (Inverter) (TOP VIEW)



FUNCTION TABLE  
(each inverter)

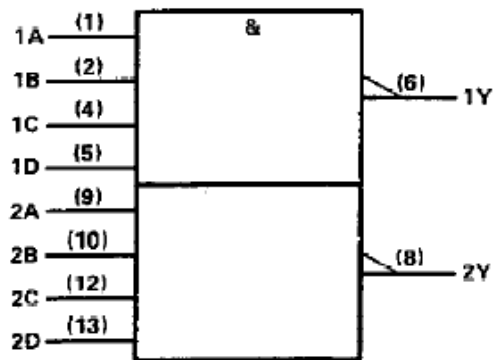
INPUT A	OUTPUT Y
H	L
L	H

## 74LS20 (And) (TOP VIEW)

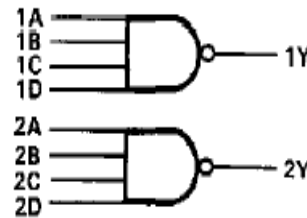


FUNCTION TABLE (each gate)

INPUTS				OUTPUT
A	B	C	D	Y
H	H	H	H	L
L	X	X	X	H
X	L	X	X	H
X	X	L	X	H
X	X	X	L	H



logic diagram



positive logic  $Y = \overline{A \cdot B \cdot C \cdot D}$  or  $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D}$

## Design and Procedure

**Working of a Circular Counter:** The circular counter increments from 0 to 15 decimal. In binary this is represented as 0000 to 1111. The counter is triggered by the input off of the clock (pin 2) cycling from high-to-low and then back from low-to-high. A buffered clock input triggers the four flip-flops on the rising edge of the clock input waveform. For proper operation of the counter, it is necessary to realize that load (pin 9) uses negative logic. In other words, to prevent the data off of A,B,C, and D (pins 3 through 6) being loaded into the buffers on the next clock cycle, load should be set high. Allowing

load to go low or to float might cause improper operation of the timer due to erroneous loading of values, thus setting the counter to a different state than is desired.

### Truth Table

A=0 Qa=0  
 B=0 Qb=0  
 C=0 Qc=0  
 D=0 Qd=0

A=1 Qa=1  
 B=1 Qb=1  
 C=1 Qc=1  
 D=1 Qd=1

There is a very useful relationship between the clock frequency and those of Qa, Qb, Qc, and Qd to understand. If the frequency of the clock is 16 Hz, then the frequency of the output from Qd is 8 Hz, Qc is 4 Hz, Qb is 2 Hz, and Qa is 1 Hz. This can be rewritten into the form of equations.

$$f_{Qd} = 0.0625 \times \text{clk}$$

$$f_{Qc} = 0.125 \times \text{clk}$$

$$f_{Qb} = 0.25 \times \text{clk}$$

$$f_{Qa} = 0.5 \times \text{clk}$$

### **11 Recognition Function**

$$f(Qd, Qc, Qb, Qa) = Qd \cdot Qc \cdot Qb \cdot Qa$$

		QdQc			
QbQa	00	01	11	10	
00	0	0	0	0	
01	0	0	0	0	
11	0	1	0	0	
10	0	0	0	0	

### **Implementation and Working of the 3 to 11 Counter**

A 3 to 11 counter can easily be implemented now that we know how to recognize when 11 is output. When the output is 11, we need to set the load pin low and output the bit pattern for decimal 3, 0011 binary.

### Verification

### Graphs

## Conclusion